IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

**[0001]** This application is a continuation of application Serial ~~No.~~No. 09/759,499, filed January 12, 2001, ~~pending~~ now U.S. Patent 6,597,619, issued July 22, 2003.

IN THE CLAIMS:

Claims 1-8 have been amended herein. All of the pending claims 1 through 8 are presented below. This listing of claims will replace all prior versions and listings in the application. Please enter these claims as amended.

1. (Currently Amended) A memory device, comprising:

a memory array for storing at least one data bit and configured to electrically operate from a power supply voltage; and

a circuit configured to receive an external reference voltage and generate in response thereto an internal reference voltage independent of ~~said~~the power supply voltage, ~~said~~the internal reference voltage for accessing and evaluating ~~said~~the at least one data bit in ~~said~~the memory array.

2. (Currently Amended) The memory device of claim 1, further comprising data input/output circuitry coupled to ~~said~~the memory array and further coupled and responsive to ~~said~~the internal reference voltage of ~~said~~the circuit.

3. (Currently Amended) The memory device of claim 1, further comprising an address register coupled and responsive to ~~said~~the internal reference voltage of ~~said~~the circuit.

4. (Currently Amended) The memory device of claim 1, wherein ~~said~~the internal reference voltage generated by ~~said~~the circuit tracks follows the ~~said~~ external reference voltage.

5. (Currently Amended) The memory device of claim 1, wherein ~~said~~the circuit comprises a following circuit configured to generate an internal reference voltage that is dependent upon ~~an~~ the external reference voltage.

6. (Currently Amended) The memory device of claim 1, wherein ~~said~~the circuit comprises a voltage follower configured to receive ~~said~~the external reference ~~signal~~ voltage at an input and ~~configured~~ to generate in response thereto ~~said~~the internal reference ~~signal~~ voltage.

7. (Currently Amended) The memory device of claim 1, wherein ~~said~~the circuit comprises a plurality of voltage followers serially coupled to receive ~~an~~ the external reference voltage and generate in response thereto ~~an~~ the internal reference voltage.

8. (Currently Amended) The memory device of claim 1, further comprising circuitry for configuring ~~said~~the memory device as one of a DRAM, SDRAM, Rambus memory, double data rate memory and flash memory.

## REMARKS

No new matter has been added. The amendments to the claims address typographical and spelling errors, and improve antecedent basis. The amendments do not affect, or surrender, any scope of any claim as originally filed.

The Applicants again request entry of the amendments as set forth herein prior to examination of the application on the merits.

Respectfully submitted,

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Date: October 21, 2003

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